# III B. Tech I Semester Supplementary Examinations, May - 2016 <br> LINEAR IC APPLICATIONS <br> (Common to ECE, EIE and ECompE) 

Time: 3 hours
Max. Marks: 70

Note: 1. Question Paper consists of two parts (Part-A and Part-B)<br>2. Answering the question in Part-A is compulsory<br>3. Answer any THREE Questions from Part-B<br>*****

## PART - A

1 a) Define slew rate. What causes it?
[4M]
b) Compare the frequency response of compensated and uncompensated op-amp.
c) Give some limitations of op-amp as a comparator.
d) Why do we use higher order filters? Give the relationship between order of a filter [4M] and roll off rate.
e) Define capture range and lock in range of a PLL.
f) What is an all-pass filter? Mention some of its applications.

## PART -B

2 a) Perform AC and DC analysis of an emitter coupled pair.
b) Draw the circuit of any one type of differential amplifier and explain the operation.

3 a) Draw and explain the three open loop op-amp configurations with neat circuit diagram.
b) Explain the frequency compensation techniques of an Op-Amp.

4 a) What are the two closed loop configurations of an Op-Amp, obtain the gains in both the cases.
b) Draw the frequency response curve of a differentiator. How is it modified when a small resistor is connected in series with the capacitor?

5 a) Design a first order wide band reject filter with a higher cutoff frequency of 100 Hz and a lower cutoff frequency of 1 kHz . Calculate the Q of the filter.
b) Explain how a four quadrant multiplier be obtained from single quadrant multiplier.

6 a) Explain the block diagram of PLL emphasizing the capture range and lock range.
b) Design monostable multivibrator using 555 timer to produce a pulse width of [8M] 100 m sec .

7 a) Describe the operation of dual slope $A / D$ converter with necessary diagrams. Give some of its advantages \& disadvantages.
b) How many resistors are required for an 8 -bit weighted resistors D/A converter? What are those resistor values, assuming the smallest resistance is R?

